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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,068	03/19/2001	Laurence H. Cooke	262/043	9013

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BINGHAM, MCCUTCHEN LLP
THREE EMBARCADERO, SUITE 1800
SAN FRANCISCO, CA 94111-4067

EXAMINER	
THOMPSON, ANNETTE M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/812,068	COOKE ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37.CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' Amendment has been examined and remarks carefully considered. Claims 2, 7, 13, and 18 are amended. Claims 2-23 are pending.

2. Applicants' Amendment is sufficiently persuasive to obviate the outstanding objections. The pertinent rejections of the prior office action are incorporated herein.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Rejection of Claims 2-23

5. **Claims 2-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al., U.S. Patent 6,175,948 ("Miller") and the Herbert Dawid et al. paper (Dawid paper") entitled ADPCM Codec: From System Level Description to versatile HDL Model.

Miller discloses a methodology and apparatus for designing a waveform compiler, a Digital Signal Processor (DSP) type of model (see Miller, col. 5, ll. 50-57 and col. 6, ll. 10-13). Although one of ordinary skill in the art should recognize that a power analysis would be part of a DSP design methodology, Miller does not explicitly disclose a power analysis step. The Dawid paper discloses a common DSP system design methodology and environment (see Dawid, page 459, Figure 1, which details the DSP design methodology) and explicitly discloses the necessary power analysis considerations. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use or reference the DSP design methodology disclosed in the Dawid paper for further detailed disclosure or information regarding the DSP design methodology used in Miller. In this Office Action, the cites reference the Miller '948 patent unless the Dawid paper is specifically indicated.

6. Pursuant to claim 2 which recites [a] method for designing a derivative circuit block (col. 5, ll. 41-44 discloses reuse programming as a primary goal and a derivative circuit block, as disclosed by Applicants, is a reusable circuit block) comprising selecting an original circuit design (the waveform compiler, col. 5, ll. 50-57), wherein the original circuit design comprises one or more programmable fabrics (new library building blocks, col. 5, ll. 58-62); performing front-end acceptance testing on the circuit design (col. 5, line 58 to col. 6, line 5), wherein front-end acceptance comprises collecting data on a designer's available experiences (col. 5, ll. 54-57; col. 7, ll. 13-15) and acceptable degree of risk (col. 5, ll. 27-30); planning a chip layout (col. 6, ll. 6-10); programming at

least one of the one or more programmable fabrics (col. 6, ll. 10-19) and performing verification of the derivative circuit block (col. 6, ll. 45-50).

7. Pursuant to claim 3, wherein planning the chip layout does not result in altering the chip layout (col. 6, ll. 6-16).

8. Pursuant to claim 4, further comprising performing clocking and timing analysis prior to the step of performing verification of the derivative circuit block (see Fig. 9, step 910; also col. 13, line 67 to col. 14, line 11.

9. Pursuant to claim 5, further comprising the step of performing power analysis prior to the step of performing verification of the derivative circuit block (*Dawid's* Figure 1 illustrates a power analysis (*Dawid's* "power consumption") prior to verification.

10. Pursuant to claim 6, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified (col. 7, line 64 to col. 8, line 9 suggests this limitation)

11. Pursuant to claim 7, wherein (a) through (e) are repeated to design a second derivative design: col. 17, line 55 to col. 18, line 27 suggest this limitation (e.g. "modules can be added" and "user library component creation".

12. Pursuant to claim 8, wherein planning the chip layout comprises analyzing timing requirements (col. 4, ll. 24-30; see also col. 17, ll. 8-12) to ensure the derivative circuit block meets all applicable timing requirements.

13. Pursuant to claim 9, further comprising assembling the chip layout col. 6, ll. 51-53 suggests this step of completion (i.e. "the design is ready for the target implementation).

14. Pursuant to claim 10, wherein the original circuit design further comprises one or more non-programmable fabrics (existing library building blocks, col. 5, ll. 58-62).

15. Pursuant to claim 11, wherein the one or more programmable fabrics each has a port access and hierarchical routing (col. 10, ll. 1-8 and ll. 15-27 disclose the use of FPGAs which Applicants have disclosed (specification, page ¶ 120) as a programmable fabric with inherent programming access and hierarchical levels).

16. Pursuant to claim 12, further comprising determining a power level for each programmable fabric and each non-programmable fabric through simulation (the *Dawid* paper, page 464, Figure 5 illustrates this limitation).

17. Pursuant to independent claim 13 and dependent claims 14-23, these claims respectively address the method limitations already considered and rejected in independent claim 2 and dependent claims 3-12, respectively and additionally recites a computer readable medium for executing the claimed method. The use of database systems as disclosed by Miller (col. 15, ll. 47-67) and the Dawid paper for implementing a DSP design methodology necessarily includes the use of computer readable media. Therefore, claims 13-23 are likewise rejected based on the rationale outlined in claims 2-12, supra.

Remarks

18. Upon reconsideration and based upon Applicant's remarks Examiner has considered in entirety the limitation of "front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprises collecting data on a designer's available experiences and acceptable degree of risk." As cited supra, and

mentioned in the Remarks section of the non-final office action, Miller also discloses consideration of risk reduction at column 5, lines 27-30. Therefore, Miller does at least suggest if not outright disclose the limitation of front-end acceptance. Accordingly, the rejection of claims 2-23 under 35 U.S.C. 103 (a) is maintained.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562 or the Customer Service Center whose telephone number is (571) 272-1750.

21. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

A. M. THOMPSON
Primary Examiner
Technology Center 2800